CLAIMS

What is claimed is:

1. A method of forming a semiconductor device, the method comprising the steps of:

forming a dielectric layer over a substrate;

forming a mask layer over the dielectric layer;

patterning the mask layer to form a mask including a mask line and space pattern, the mask line and space pattern including at least one mask space; and

forming a conductive layer in the at least one mask space, the conductive layer including a width dimension about equal to the width dimension of the least one mask space.

2. The method according to claim 1, further comprising the steps of:

removing the mask to expose sidewalls of the conductive layer, wherein the sidewalls include relatively smooth surfaces.

3. The method according to claim 1, wherein the mask layer comprises at least one of photoresist; silicon oxide (Si_xO_y), silicon-dioxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$, $BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), PMN ($PbMg_xNb_{1-x}O_3$), binary and tertiary metal oxides, other metal oxides; silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), other nitrides; zirconium silicate, hafnium silicate, other silicates; ferro electric material; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous, single crystal, polycrystalline, or nanocrystalline form; and mixtures thereof.

4. The method according to claim 1, further comprising the step of:

forming and patterning an anti-reflective coating (ARC) over the mask layer.

5. The method according to claim 4, wherein the mask comprises the patterned ARC and the patterned mask layer.

6. The method according to claim 1, wherein the dielectric layer comprises a gate dielectric layer.

7. A method according to claim 6, wherein the semiconductor device comprises;

a gate stack formed on the substrate including an active layer interposed between a source and a drain, the gate stack including:

the gate dielectric layer disposed over the substrate; and

the conductive layer disposed over the gate dielectric layer.

8. A method according to claim 7, wherein the gate dielectric layer includes a gate dielectric material including a permittivity greater than a permittivity of silicon-dioxide (SiO_2).

9. The method according to claim 1, wherein the substrate comprises

a germanium-on-insulator (GOI) structure including:

a semiconductor substrate;

an insulating layer disposed over the semiconductor substrate; and

a semiconductive layer comprising germanium (Ge) disposed over the insulating layer.

10. The method according to claim 9, wherein the germanium (Ge) comprises crystalline germanium.

11. The method according to claim 10, wherein the dielectric layer comprises a charge-trapping dielectric layer.

12. The method according to claim 11, wherein the charge-trapping dielectric layer includes:

a tunneling layer;

a charge-trapping layer; and

an insulating layer;

wherein the tunneling layer is disposed over the substrate, the charge-trapping layer is disposed over the tunneling layer and the insulating layer is disposed over the charge-trapping layer.

13. The method according to claim 1, wherein the dielectric layer comprises at least one of silicon oxide (Si_xO_y), silicon-dioxide (SiO_2), aluminum oxide (Al_2O_3), hafnium oxide (HfO), zirconium oxide (ZrO), titanium oxide (TiO), yttrium oxide (YO), lanthanum oxide (La_2O_3), cerium oxide (CeO_2), bismuth silicon oxide ($Bi_4Si_2O_{12}$), tantalum oxide (Ta_2O_5), tungsten oxide (WO_3), $LaAlO_3$, BST ($Ba_{1-x}Sr_xTiO_3$), $PbTiO_3$, $BaTiO_3$, $SiTiO_3$, $PbZrO_3$, PST ($PbSc_xTa_{1-x}O_3$), PZN ($PbZn_xNb_{1-x}O_3$), PZT ($PbZr_xTi_{1-x}O_3$), PMN ($PbMg_xNb_{1-x}O_3$), binary and tertiary metal oxides, other metal oxides; silicon nitride (Si_xN_y), silicon oxynitride (SiO_xN_y), other nitrides; zirconium silicate, hafnium silicate, other silicates; ferro electric material; the aforementioned materials implanted with any element; the aforementioned materials in layered or graded composition combinations; the aforementioned materials in porous, amorphous, single crystal, polycrystalline, or nanocrystalline form; and mixtures thereof.

14. The method according to claim 1, wherein the mask defines a pitch of the mask line and space pattern.

15. The method according to claim 2, wherein the step of forming the conductive layer comprises the steps of:

forming a conformal layer of a conductive material over the mask and exposed surface of the dielectric layer; and

anisotropically etching to remove a portion of the conductive material from horizontal surfaces of the mask.

16. A method of forming a semiconductor device, the method comprising the steps of:

forming a mask over a substrate to include a line and space pattern, the line and space pattern having at least one space including a width dimension; and

forming a conductive layer in the at least one space of the mask, the conductive layer includes a width dimension about equal to the width dimension of the at least one space of the mask.

17. A semiconductor device, comprising:

a substrate;

a dielectric layer disposed over the substrate; and

a conductive layer disposed over the dielectric layer,

wherein the conductive layer comprises a line and space pattern and wherein sidewalls of the conductive layer include relatively smooth surfaces.